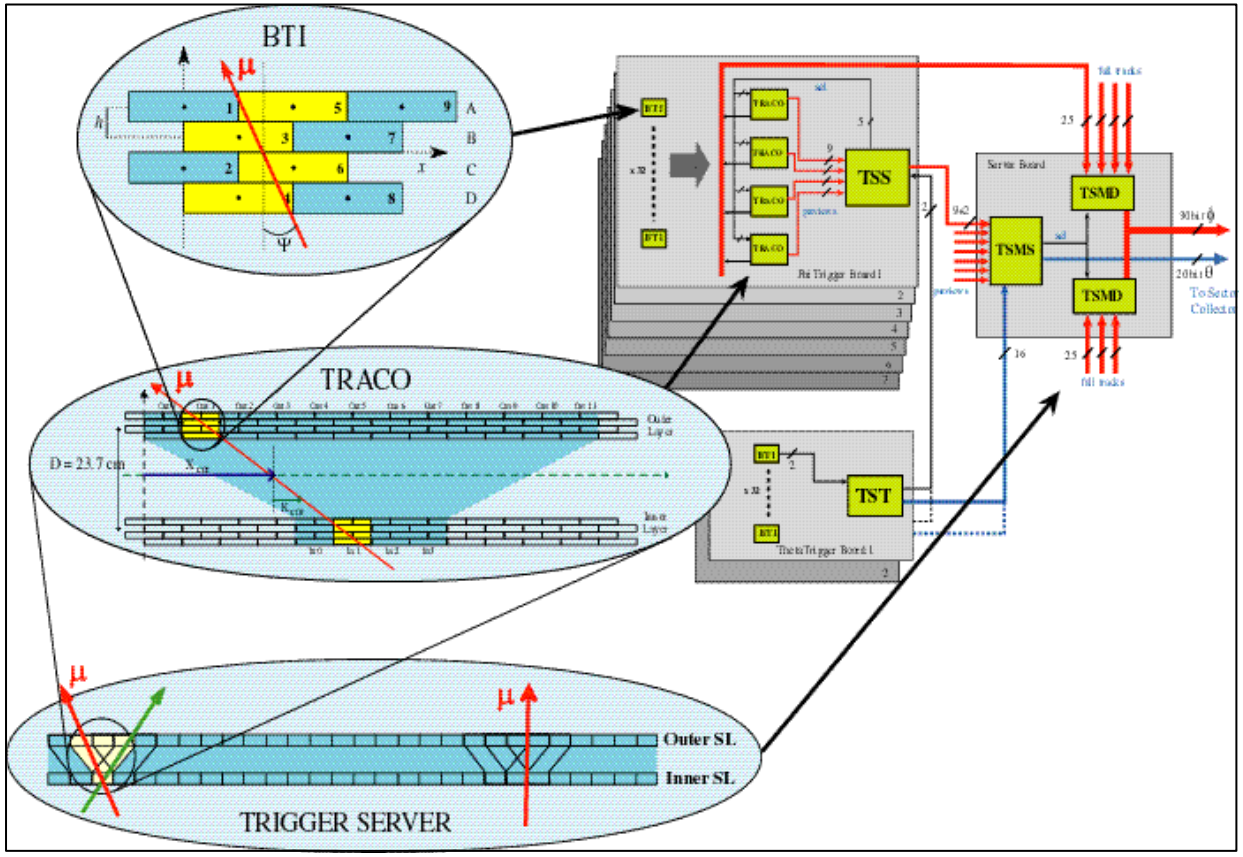
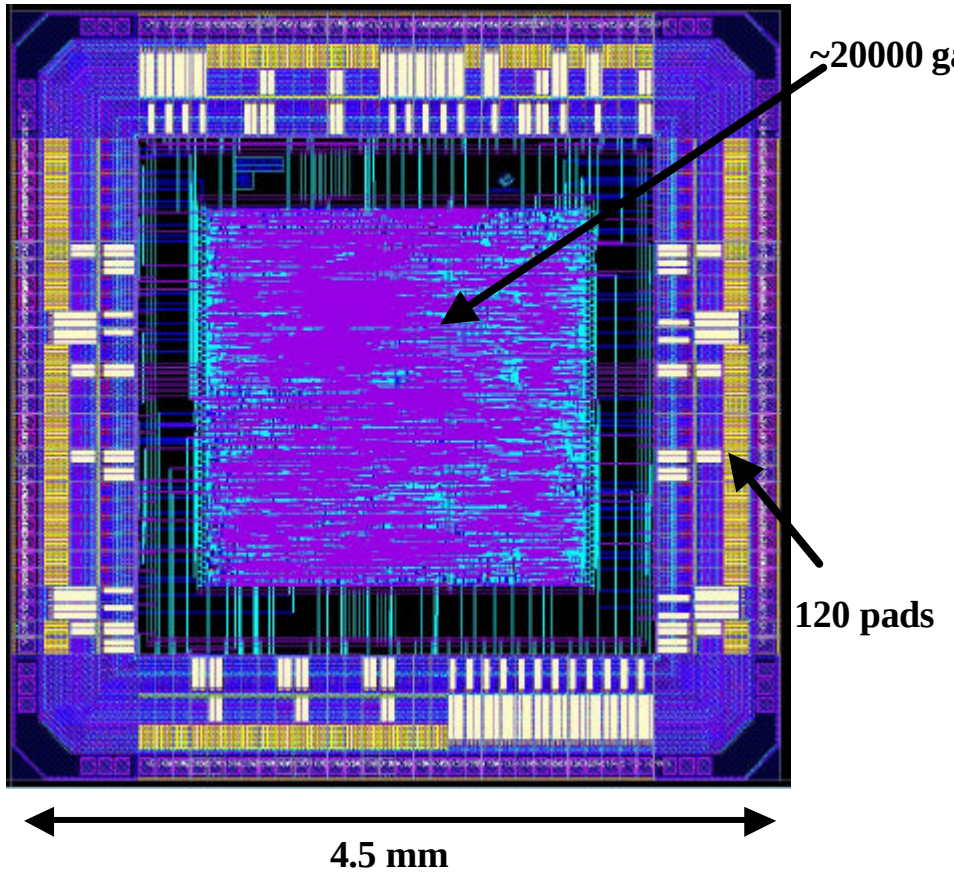
DT Trigger Server status



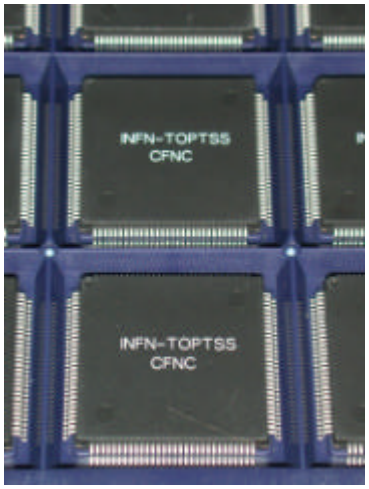
Reminder:

- two stage system on chamber;
- 1080 Track Sorter Slave (TSS): ASIC devices;
- 250 Track Sorter Master (TSM): each of them composed by 3 pASIC chips.

TSS: ASIC prototype



• Final prototype received on 10th August :



10 ceramic,
30 plastic package

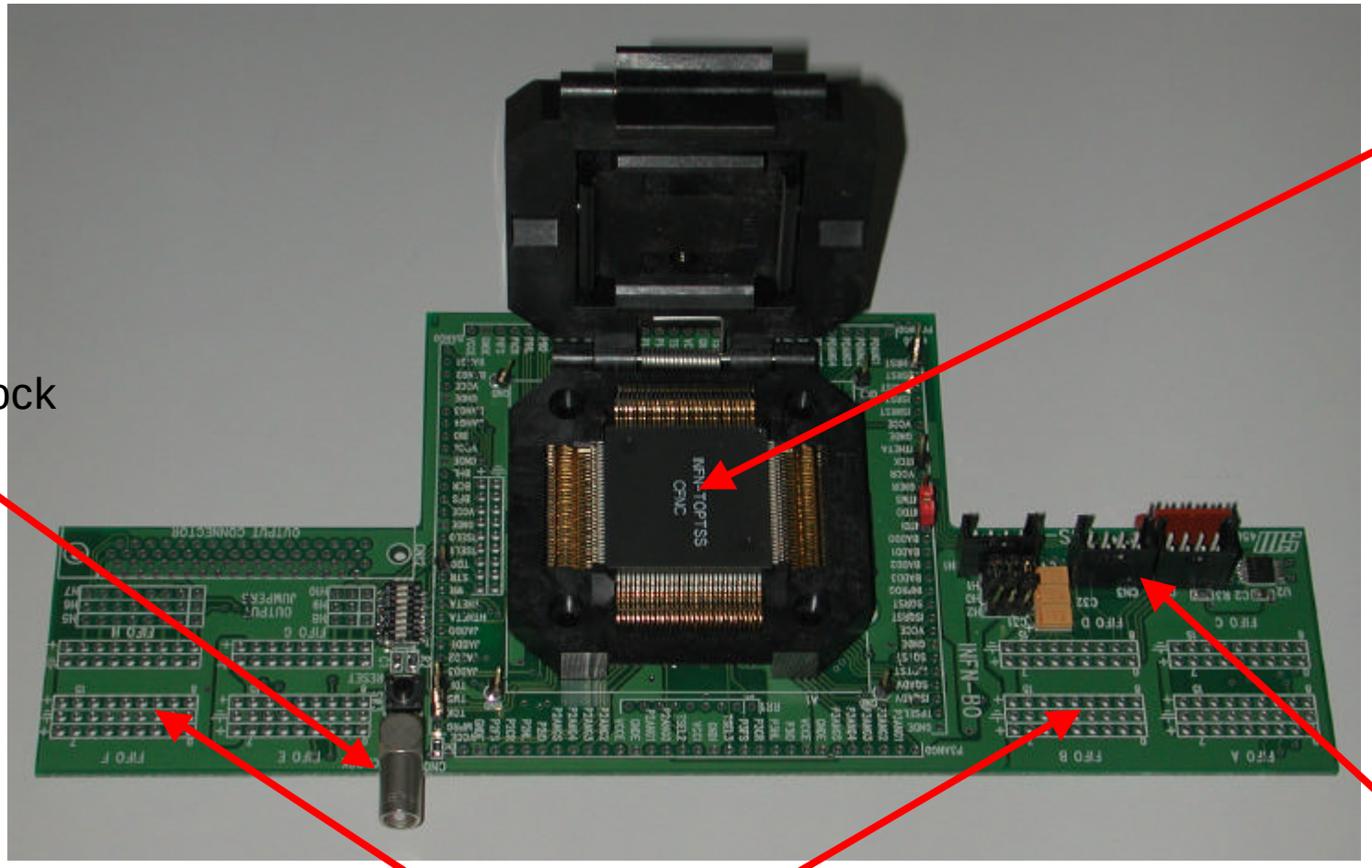
- CMOS 0.5 µm Alcatel
  (via Europractice: low cost!)

- full JTAG control

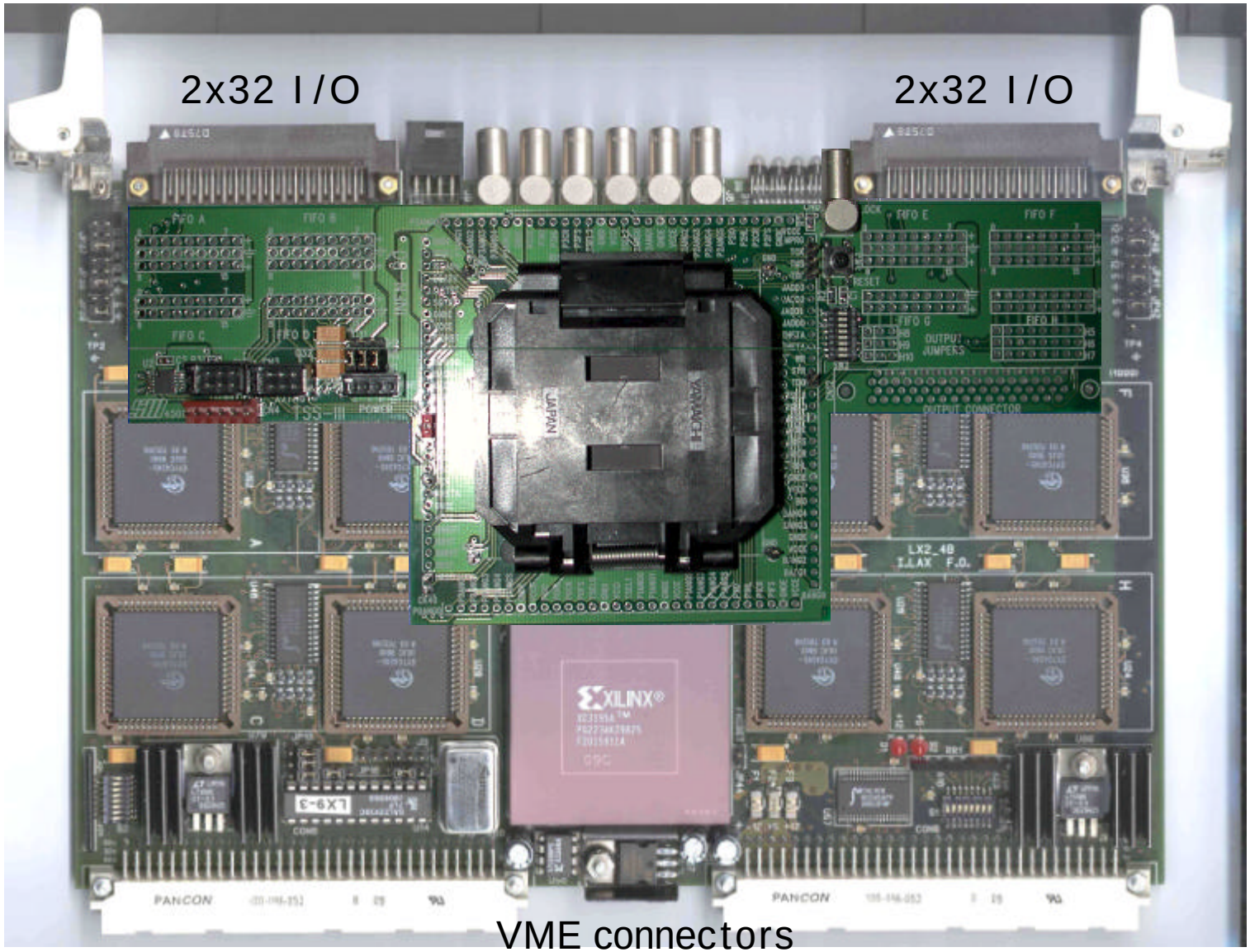
- built-in test features

• reference manual almost ready
  (CMS internal note)

Test tools


DUT
40 MHz clock
91 I/O @ 40 MHz: use Pattern Unit..
hardware ready, software almost ready
JTAG access:
tested ok

Test tools



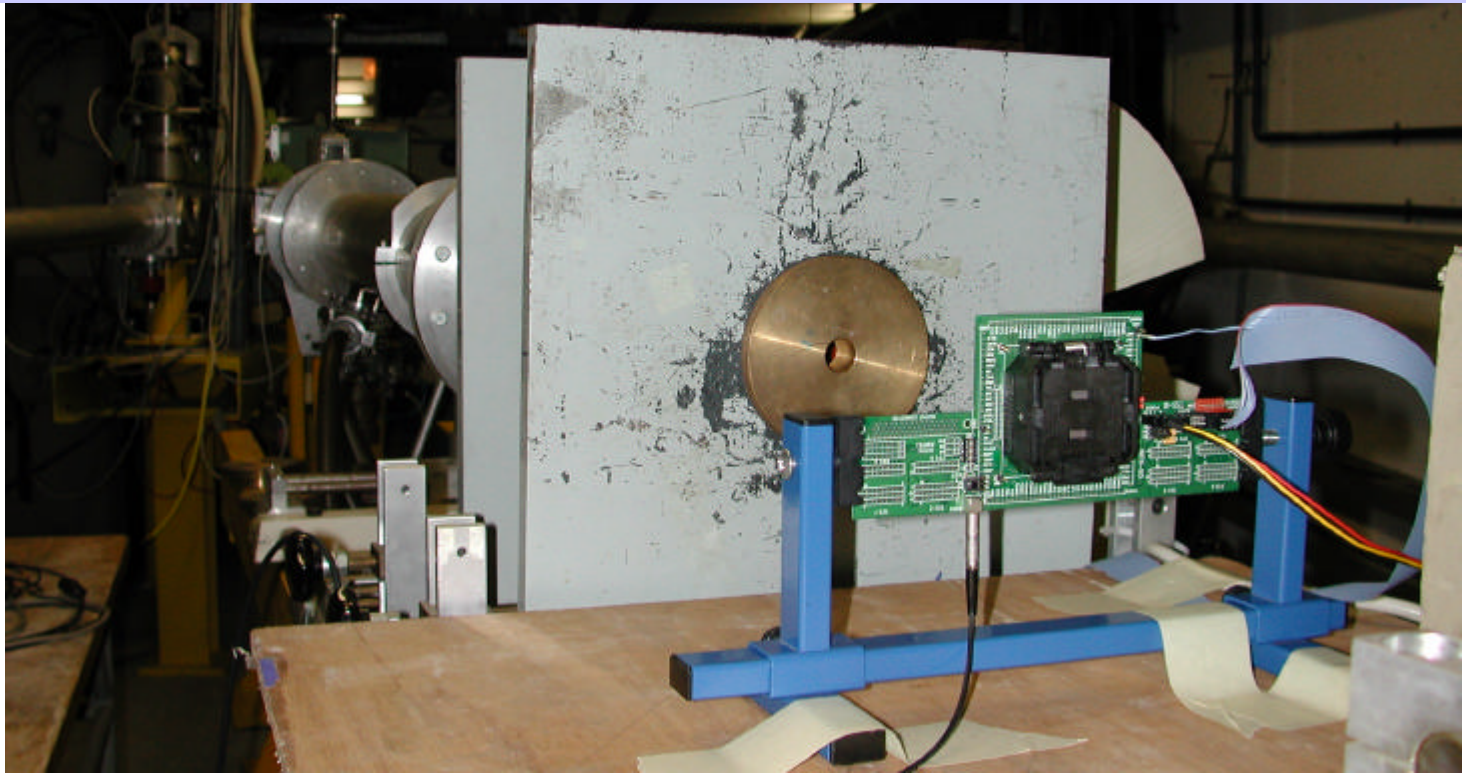
Pattern Unit:

128 channels
up to 80 MHz

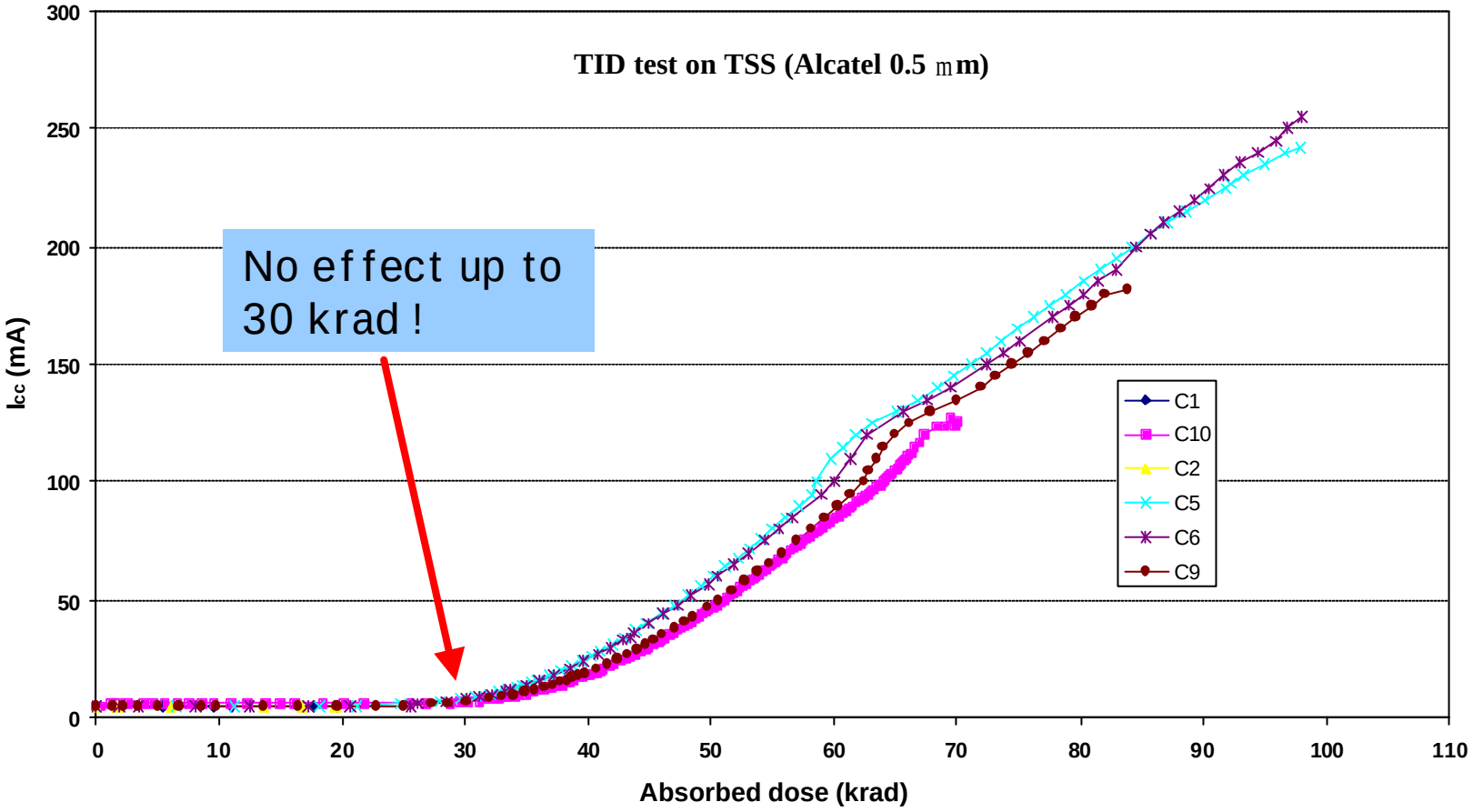
Irradiation tests on TSS: CRC

6 prototypes irradiated at CRC Louvain: 60 MeV protons
total fluence: 2.8×10^{12} p/cm^2
total equivalent dose: 389 krad

Expected in Muon Barrel (in 10 years): >20 MeV neutron fluence: 1.0×10^{9} n/cm^2
total dose: 0.01 krad



Irradiation tests on TSS: TID



Irradiation tests on TSS: SEE

Chip	Dose (krad)	#SEE (<30krad)	#SEE (>30krad)
C10	70	0	0
C9	84	0	**2**
C5	98	0	**2**
C6	98	**1**	**1**
C1	19.6	0	0
C2	19.6	0	0

Chain of 256 FFs monitored through JTAG circuitry

Six SEE after 386 krad

$\sigma_{SEU} = 2.3 \times 10^{-15}$ cm^2/bit

More events after
30 krad threshold..!?!

TSS production

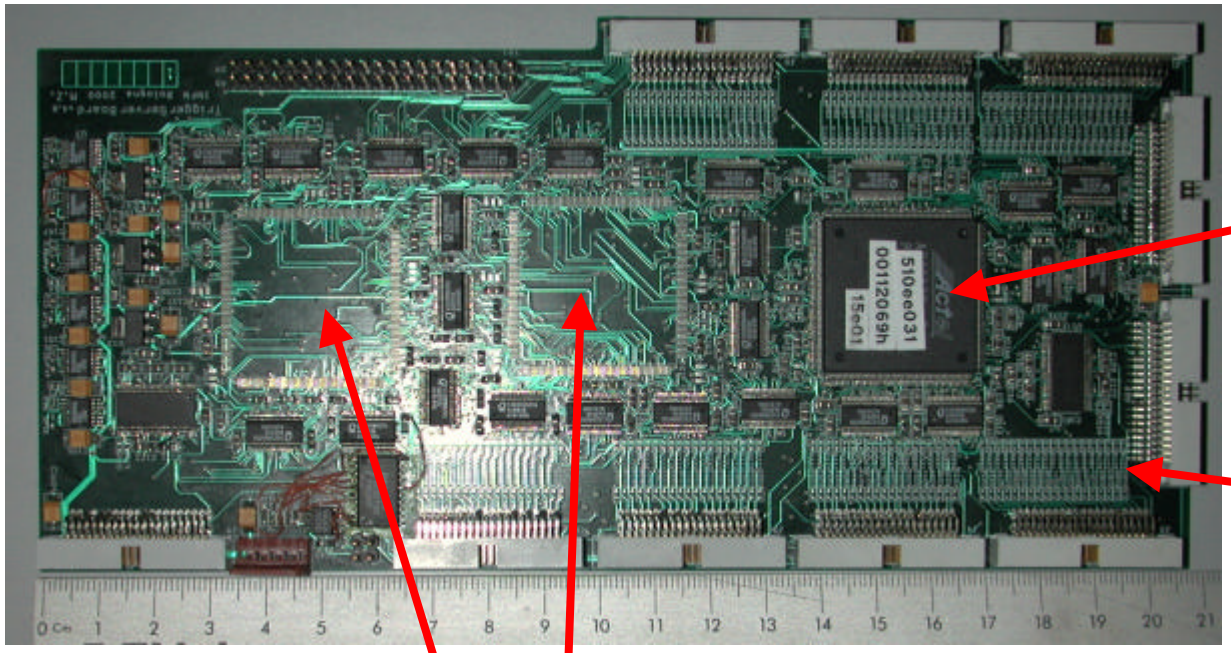
- Irradiation test was ok (through JTAG)
- still to be completed the test at 40 MHz

- ready to start production and test of 1500 pieces at the end of 2001
- we will use Small Volume Production with Europractice (reduced cost mask set);
- the test of chips will be done at home.

We are on schedule with milestones:

DT	TSS ASIC	Production start	Dec-01
DT	TSS ASIC	Begin Delivery	Jan-02
DT	TSS ASIC	Production done	Apr-02

Track Sorter Master (pASIC)

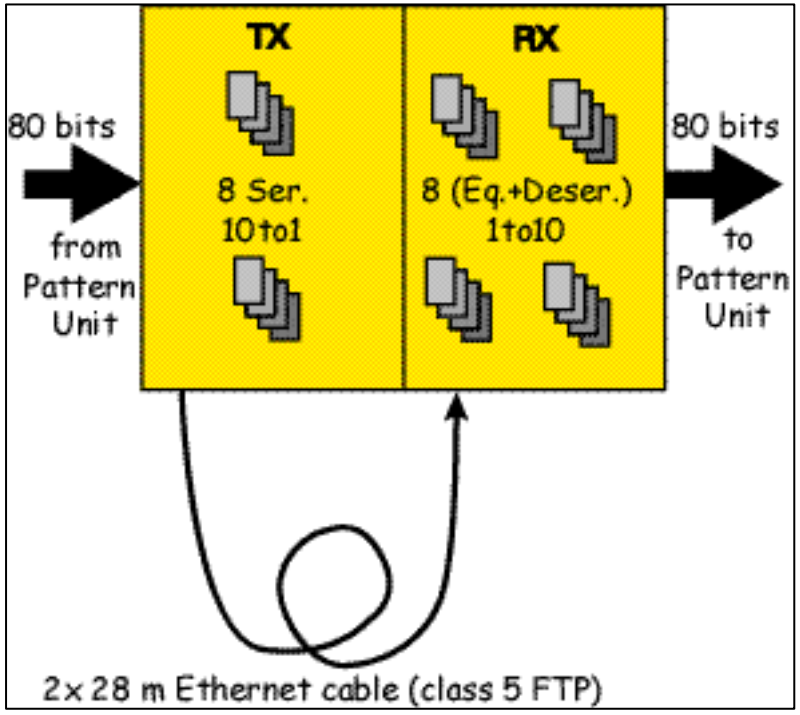


- Received 900 chips from Actel
- TSMS programming ready
- TSMD in simulation phase: programming test in Nov 2001
- Server Board (TSM side) electrical schemes ready: wait for integration test with Controller components to be placed on the other side.

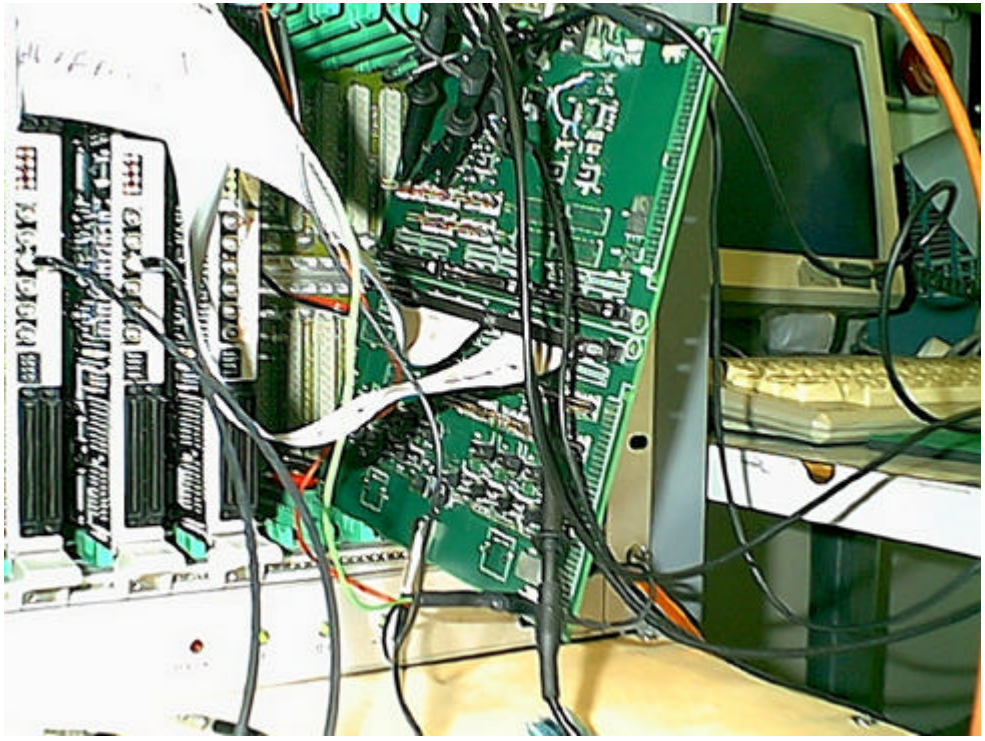
On schedule with milestones:

DT	TSMS, TSMD, PASICs	Production start	Jul-01
DT	TSMS, TSMD, PASICs	Begin Delivery	Jan-02
DT	TSMS, TSMD, PASICs	End Delivery	Apr-02

LVDS trigger link test

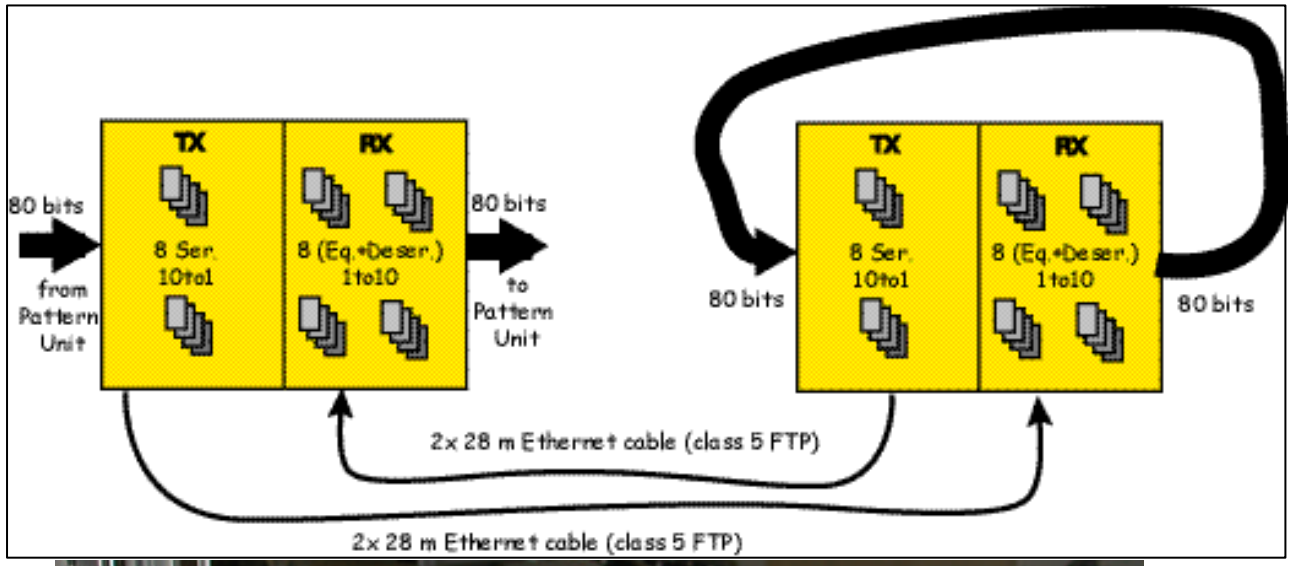


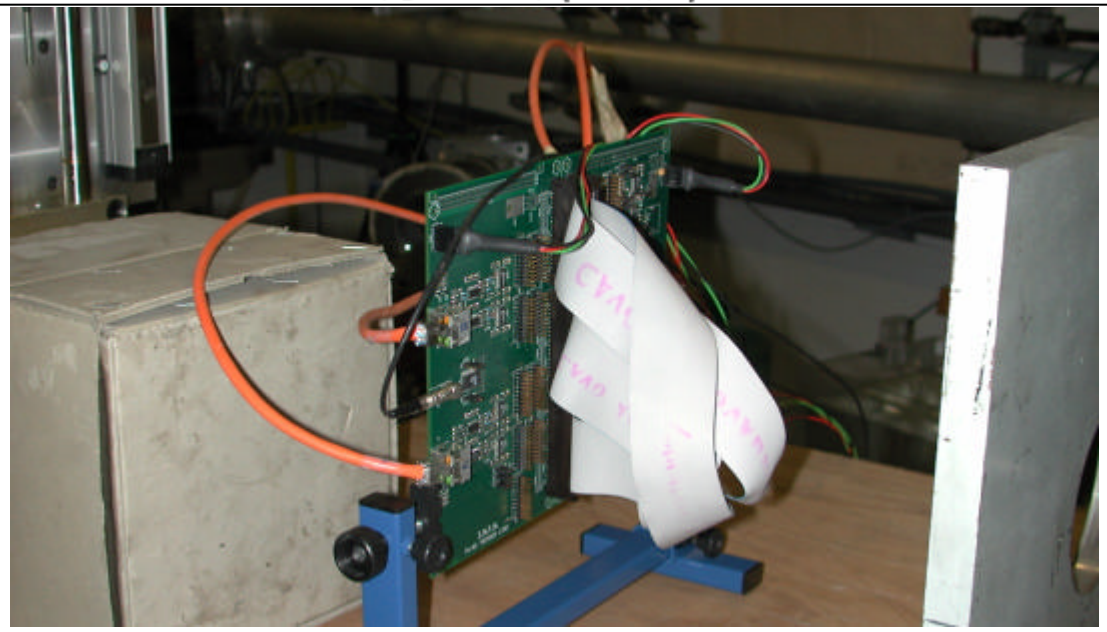
@ 30 MHz: 3×10^{-11} errors/bit
@ 40 MHz: 1×10^{-9} errors/bit



Preliminary

Irradiation tests on Trigger Links





Devices irradiated up to 80-90 krad without damages

SEE under study..but seems negligible:

2.4×10^{-9} errors/bit @ 40 MHz

Preliminary