

SPD Project Status

G. Stefanini/CERN-EP

- Submissions
- Bump-bonding trials
- Access to 0.25um process products
- Detectors

Pixel chip, 6 metal layers

Engineering run: lot of 6 wafers (nominal lot size)

Out of foundry on Monday 18 Sept

Delivery to CERN through IBM Burlington (USA)

- immediate delivery: 2 wafers without back-side grinding (BSG)
- rest on hold until confirmation of thickness following bump deposition trials on dummy wafers

Expect to start lab test end Sept

Low-cost, top metal layer only

Pattern (“snake”) for bump-bonding trials

Production run: lot of 24 wafers total quantity

Out of foundry on Monday 11 Sept

Delivery to CERN through IBM Burlington (USA)

- 12 wafers without back-side grinding (BSG) thickness 750um
- 12 wafers with back-side grinding (BSG) thickness 300um

Expect delivery to CERN in the next few days

Key issues

- Processing 8” wafers after BSG
- Thinning (BSG) of wafers after bump deposition
- Yield in production

Test and optimise vendor process using low-cost dummy wafers

Three vendors contacted so far

process and current capability

- | | | | |
|--------------------------------|---------|--------------|----|
| – Alenia Marconi Systems (AMS) | Italy | Indium bumps | 6” |
| – VTT | Finland | solder | 6” |
| – IZM | Germany | solder | 8” |

Quotes

- AMS details under discussion, upgrade of 6” facility to 8” funded by INFN
- VTT received
- IZM still waiting

Other possible sources

- Vendor in USA with 8” capability (solder bumps)

- Phase 1 Oct/Nov 00
- Test vendor’s handling equipment using raw wafers (no metal layer)
 - 60 raw wafers already delivered to CERN (50 with BSG, 10 without BSG)
 - Process quarters of dummy wafers

- Phase 2 Nov/Dec 00
- Complete tests with dummy wafers
 - Process quarters of pixel chip wafers

- Phase 3 Q1/01
- Process 6” central region of dummy wafers (AMS, VTT)
 - Process full 8” dummy wafer (IZM, VTT)
 - Process full 8” pixel wafer (IZM)

- Phase 4 Q2/01
- Process full 8” pixel wafer all vendors

Test flip-chip assemblies on carrier bus Q1/01

Beam test of flip-chip assemblies Q2/01

Pixel wafer production run June/July 01

1

Already granted to Institutes in EU countries

Now extended to Slovakia (Bratislava and Kosice)

This applies to temporary export of assemblies, modules, etc for testing purposes

Wafers 5"

Thickness 300um

- 12 dummy wafers (pixels on SiO₂ passivation layer openings) done
- for bump-bonding trials
- 15 detector wafers (pixels on junction side) ?

Thickness 200um

- 2 detector wafers ?

Some confusion in submission, modification and follow-up of orders

- *how to avoid that in the future...*